

# SoC Blockset™ Release Notes



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## *SoC Blockset™ Release Notes*

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**Version: 1.0**

**New Features**

## **Introducing SoC Blockset: Design, evaluate, and implement SoC hardware and software architectures**

SoC Blockset™ provides Simulink® blocks and visualization tools for modeling, simulating, and analyzing hardware and software architectures for ASICs, FPGAs, and systems on a chip (SoC). You can build your system architecture using memory models, bus models, and I/O models, and simulate the architecture together with the algorithms.

SoC Blockset lets you simulate memory and internal and external connectivity, as well as scheduling and OS effects, using generated test traffic or real I/O data. You can quickly explore different system architectures, estimate interface complexity for hardware and software partitioning, and evaluate software performance and hardware utilization.

SoC Blockset exports reference designs for Xilinx® and Intel® FPGA devices and SoC platforms, including Zynq®-7000, UltraScale+™, and Intel SoC FPGAs. These reference designs can be used with Xilinx and Intel design tools.

### **SoC Blockset Support Package for Xilinx Devices: Generate, build, and deploy reference designs on Xilinx devices**

The SoC Blockset Support Package for Xilinx Devices with Embedded Coder® or HDL Coder™ can export reference designs for Xilinx FPGA devices and SoC platforms. These reference designs can be used with Xilinx design tools.

The support package helps to automate integration, execution, and verification of reference designs for the SoC platforms, including Xilinx Artix®-7, Xilinx Kintex®-7, XilinxZynq, and XilinxZynqUltraScale+.

### **SoC Blockset Support Package for Intel Devices: Generate, build, and deploy reference designs on Intel devices**

The SoC Blockset Support Package for Intel Devices with Embedded Coder or HDL Coder can export reference designs for Intel FPGA devices and SoC platforms. These reference designs can be used with Intel design tools.

The support package helps to automate integration, execution, and verification of reference designs for the SoC platforms, including Intel Arria® 10 and Intel Cyclone® V.